```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;   selected revisions: 18
description:
top level BOM
----------------------------
revision 3.703
date: 1995/05/12 03:50:36;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/baseplate

REbuild with new power assignments in the padring

Geert
----------------------------
revision 3.702
date: 1995/05/12 02:14:19;  author: stick;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

New file - wingz spreadsheet.
----------------------------
revision 3.701
date: 1995/05/11 23:09:38;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/iq

avoid toplevel collisions
----------------------------
revision 3.700
date: 1995/05/11 22:48:00;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

avoid toplevel collisions
----------------------------
revision 3.699
date: 1995/05/11 22:46:45;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.698
date: 1995/05/11 17:19:28;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Replace another flop with orff3 so that UnbHiPriR12 is logically identical
to UnbHiPriR12a.

Present placement should work.  Retrying now.
----------------------------
revision 3.697
date: 1995/05/11 00:53:36;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at
```

Here's the change:

```
< ff_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11)                        ,DB(nbCinR12,
4) );
---
> /* or in D(vldSN128WrtIR11),D(vldSN64WrIQR11) terms to make these cases high
priority */
> orff3_1 UnbHiPriR12 ( A(phi) ,nbHiPriR11 ,vldSN128WrtIR11 ,vldSN64WrIQR11
,DB(nbCinR12,    4) );
```

The idea is to make vldSN128WrtI and vldSN64WrIQ high priority so they don't
get dropped on the floor in nb. Changed no instance names, so present placement
may work.

Seems to have gotten thru pass2 OK, so I'm releasing it.
----
revision 3.696
date: 1995/05/10 18:50:18; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

attempt to solve top-level routing problems.
----
revision 3.695
date: 1995/05/10 13:33:16; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

this version fully places at the top level
----
revision 3.694
date: 1995/05/09 21:04:55; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisons with xlu
----
revision 3.693
date: 1995/05/09 18:12:21; author: vo; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
        Makefile.tst

Yesterday change to srf rule for the fence wire was messed up . This version
fixed the problem .
----
revision 3.692
date: 1995/05/09 02:29:14; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Makefile.tst:
        Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
        Added this file

uu/Makefile:
        Suppress warning about gdep.in

mc/Makefile:
```

```
              Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
       Updated from latest top level
---------------------------
revision 3.691
date: 1995/05/08 20:18:33;  author: vo;   state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce



Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
---------------------------
revision 3.690
date: 1995/05/08 18:24:57;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid collisions with es
---------------------------
revision 3.689
date: 1995/05/07 06:18:21;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc
      mc.power.tab.top

regenerated to reduce strengths no removed from power.tab.local
---------------------------
revision 3.688
date: 1995/05/07 02:34:44;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/ukernel

build in /u/chip
---------------------------
revision 3.687
date: 1995/05/06 17:11:18;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uu_control.pim uu/uu.power.tab.top \
euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC.  Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ.  The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC.  Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target.  For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc.  Change is to freeze ICC prblm code if target defers prblm.
---------------------------
                                    ....
```

```
revision 3.686
date: 1995/05/06 16:18:26;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Yet another placement change.  Should reduce maximum driver to pad
length from ~1.5mm to ~0.5mm.

This converges in 0 iterations with up-to-date drio.power.tab.top.
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/BOM,v
Working file: baseplate/BOM
head: 33.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 65;     selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 24.0
date: 1995/05/12 03:50:09;  author: geert;  state: Exp;  lines: +1 -1
Release Target: euterpe/baseplate

REbuild with new power assignments in the padring

Geert
----------------------------
revision 23.1
date: 1995/05/12 03:50:00;  author: geert;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/padlist.lst,v
Working file: baseplate/padlist.lst
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29;     selected revisions: 1
description:
----------------------------
revision 1.29
date: 1995/05/12 03:49:00;  author: geert;  state: Exp;  lines: +21 -21
Made the pad-switch VSS/VDD around and in the byte channel
to accomodate the sealring power change

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v
Working file: doc/cerberus.mif
head: 4.39
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 53;    selected revisions: 1
description:
----------------------------
revision 4.34
date: 1995/05/11 23:44:35;  author: bobm;  state: Exp;  lines: +280 -4274
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/clock.mif,v
Working file: doc/clock.mif
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;    selected revisions: 1
description:
----------------------------
revision 19.4
date: 1995/05/11 23:44:04;  author: bobm;  state: Exp;  lines: +105 -3258
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/endian.mif,v
Working file: doc/endian.mif
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;    selected revisions: 1
description:
----------------------------
revision 19.3
date: 1995/05/11 23:45:31;  author: bobm;  state: Exp;  lines: +388 -436
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarch.book,v
Working file: doc/euterpe-microarch.book
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
----------------------------
revision 4.11
date: 1995/05/11 23:40:35;  author: bobm;  state: Exp;  lines: +23 -14
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarchTOC.mif,v
Working file: doc/euterpe-microarchTOC.mif
```

```
head: 4.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
----------------------------
revision 4.13
date: 1995/05/11 23:40:45;  author: bobm;  state: Exp;  lines: +1500 -1043
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 4.21
date: 1995/05/11 23:43:39;  author: bobm;  state: Exp;  lines: +2402 -811
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/front.mif,v
Working file: doc/front.mif
head: 16.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
----------------------------
revision 16.7
date: 1995/05/11 23:40:39;  author: bobm;  state: Exp;  lines: +27 -35
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v
Working file: doc/intro.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 4.20
date: 1995/05/11 23:40:52;  author: bobm;  state: Exp;  lines: +777 -821
periodic checkin of review changes.  getting close now.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
--------------------------
revision 4.31
date: 1995/05/11 23:42:24;  author: bobm;  state: Exp;  lines: +2413 -5277
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
Working file: doc/newchanges.mif
head: 16.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
--------------------------
revision 16.9
date: 1995/05/11 23:45:47;  author: bobm;  state: Exp;  lines: +434 -56
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
--------------------------
revision 4.22
date: 1995/05/11 23:41:16;  author: bobm;  state: Exp;  lines: +101 -201
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 1
description:
--------------------------
revision 4.20
```

```
date: 1995/05/11 23:41:53;  author: bobm;  state: Exp;  lines: +1447 -1320
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 4.20
date: 1995/05/11 23:43:56;  author: bobm;  state: Exp;  lines: +735 -389
periodic checkin of review changes.  getting close now.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;    selected revisions: 1
description:
----------------------------
revision 4.108
date: 1995/05/07 02:34:19;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/ukernel

build in /u/chip
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/end.S,v
Working file: verify/include/end.S
head: 1.38
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 2
description:
----------------------------
revision 1.31
date: 1995/05/11 23:24:40;  author: dit00;  state: Exp;  lines: +2 -1
Include cerberus.h
----------------------------
revision 1.30
date: 1995/05/10 17:10:35;  author: claseman;  state: Exp;  lines: +80 -1
add perf_print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
```

```
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 5
description:
----------------------------
revision 1.157
date: 1995/05/12 00:30:16;  author: jeffm;  state: Exp;  lines: +2 -2
Do cache, nb, exception, and interrupt nastiness.
----------------------------
revision 1.156
date: 1995/05/10 00:06:26;  author: lisar;  state: Exp;  lines: +11 -4
New test, bashes one address in 4 spaces.
----------------------------
revision 1.155
date: 1995/05/09 20:44:20;  author: jeffm;  state: Exp;  lines: +2 -2
Test cache thrashing with different LVA[63:48] and GVA[63:48] combinations.
----------------------------
revision 1.154
date: 1995/05/09 18:18:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test stores to dram when only one or two bytes of an octlet are
non-X (done through writebacks).
----------------------------
revision 1.153
date: 1995/05/09 00:02:07;  author: jeffm;  state: Exp;  lines: +2 -2
Make sure changing the event mask can happen at any time wrt the
arrival of a rupt.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshftshort.test,v
Working file: verify/standalone/dp/dpgshftshort.test
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;    selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/05/09 21:26:46;  author: veena;  state: Exp;  lines: +9 -8
removed exception cases for immediate shift opcodes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/bgatei.S,v
Working file: verify/standalone/uu/bgatei.S
head: 6.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
----------------------------
revision 6.8
```

```
date: 1995/05/10 23:41:23;  author: jeffm;  state: Exp;  lines: +48 -14
Added checks to make sure the priv level actually changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/ex10test.S,v
Working file: verify/standalone/uu/ex10test.S
head: 7.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 7.5
date: 1995/05/07 05:19:16;  author: jeffm;  state: Exp;  lines: +21 -42
Use memory management macro.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/ex9test.S,v
Working file: verify/standalone/uu/ex9test.S
head: 7.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 7.3
date: 1995/05/07 05:22:20;  author: jeffm;  state: Exp;  lines: +3 -41
Turn on memory management with macros.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/stbash,v
Working file: verify/tools/stbash
head: 7.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 7.1
date: 1995/05/09 01:45:44;  author: lisar;  state: Exp;
Bash the specified section.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 5
```

```
description:
----------------------------
revision 1.157
date: 1995/05/12 00:30:16;  author: jeffm;  state: Exp;  lines: +2 -2
Do cache, nb, exception, and interrupt nastiness.
----------------------------
revision 1.156
date: 1995/05/10 00:06:26;  author: lisar;  state: Exp;  lines: +11 -4
New test, bashes one address in 4 spaces.
----------------------------
revision 1.155
date: 1995/05/09 20:44:20;  author: jeffm;  state: Exp;  lines: +2 -2
Test cache thrashing with different LVA[63:48] and GVA[63:48] combinations.
----------------------------
revision 1.154
date: 1995/05/09 18:18:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test stores to dram when only one or two bytes of an octlet are
non-X (done through writebacks).
----------------------------
revision 1.153
date: 1995/05/09 00:02:07;  author: jeffm;  state: Exp;  lines: +2 -2
Make sure changing the event mask can happen at any time wrt the
arrival of a rupt.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachenasty4.S,v
Working file: verify/toplevel/cachenasty4.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 35.2
date: 1995/05/10 23:43:18;  author: jeffm;  state: Exp;  lines: +3 -2
Changed comment to reflect what the test does.
----------------------------
revision 35.1
date: 1995/05/09 20:44:16;  author: jeffm;  state: Exp;
Test cache thrashing with different LVA[63:48] and GVA[63:48] combinations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachenasty5.S,v
Working file: verify/toplevel/cachenasty5.S
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/12 00:30:10;  author: jeffm;  state: Exp;
Do cache, nb, exception, and interrupt nastiness.
```

```
================================================================================
RCS file: /s6/cvsroot/euterpe/verify/toplevel/doublemctest.S,v
Working file: verify/toplevel/doublemctest.S
head: 26.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
----------------------------
revision 26.4
date: 1995/05/11 21:24:59;  author: jeffm;  state: Exp;  lines: +169 -40
Fixed test to treate a double machine check condition as another machine
check. Also - do machine checks with memory management enabled, and
make sure memory mgmnt gets turned off. Also - the first machine check
is caused by a cerberus timeout, and the second by a double exception11.
================================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/drampartial.S,v
Working file: verify/toplevel/drampartial.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;    selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/09 18:18:25;  author: jeffm;  state: Exp;
Test stores to dram when only one or two bytes of an octlet are
non-X (done through writebacks).
================================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/exmaskatomic.S,v
Working file: verify/toplevel/exmaskatomic.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 2
description:
----------------------------
revision 35.2
date: 1995/05/09 18:49:50;  author: jeffm;  state: Exp;  lines: +5 -7
Needed to clear event register after initializing the timer and timer
match registers, but before enabling interrupt 0.
----------------------------
revision 35.1
date: 1995/05/09 00:02:03;  author: jeffm;  state: Exp;
Make sure changing the event mask can happen at any time wrt the
arrival of a rupt.
================================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_Ibash.S,v
Working file: verify/toplevel/hermes_Ibash.S
head: 35.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;    selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/10 00:06:28;  author: lisar;  state: Exp;
New test, bashes one address in 4 spaces.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermesmc.S,v
Working file: verify/toplevel/hermesmc.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 1
description:
----------------------------
revision 35.2
date: 1995/05/10 00:06:30;  author: lisar;  state: Exp;  lines: +71 -38
New test, bashes one address in 4 spaces.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermesmc.hconfig,v
Working file: verify/toplevel/hermesmc.hconfig
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;    selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/09 23:45:48;  author: lisar;  state: Exp;
Error stimulus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ibuf_storeeasy.S,v
Working file: verify/toplevel/ibuf_storeeasy.S
head: 14.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 1
description:
----------------------------
revision 14.2
date: 1995/05/08 17:46:03;  author: jeffm;  state: Exp;  lines: +66 -12
```

Make it actually access the ibuffer.
===

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ifill_debug.sig,v
Working file: verify/toplevel/ifill_debug.sig
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;   selected revisions: 2
description:
----
revision 35.2
date: 1995/05/10 00:29:20; author: lisar; state: Exp; lines: +4 -4
Correct signal names
----
revision 35.1
date: 1995/05/10 00:07:37; author: jeffm; state: Exp;
Debug icache fills.
===

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 1
description:
----
revision 1.86
date: 1995/05/10 00:06:35; author: lisar; state: Exp; lines: +760 -760
New test, bashes one address in 4 spaces.
===

RCS file: /s6/cvsroot/euterpe/verify/ukernel/BOM,v
Working file: verify/ukernel/BOM
head: 8.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;   selected revisions: 2
description:
releasebom adding BOM
----
revision 7.0
date: 1995/05/07 02:34:07; author: doi; state: Exp; lines: +1 -1
Release Target: euterpe/verify/ukernel

build in /u/chip
----
revision 6.1
date: 1995/05/07 02:34:00; author: doi; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

```
===============================================================================
RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;   selected revisions: 16
description:
top level verilog BOM
----------------------------
revision 3.567
date: 1995/05/12 02:13:55;   author: stick;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc

New file - wingz spreadsheet.
----------------------------
revision 3.566
date: 1995/05/11 23:09:18;   author: dickson;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc/iq

avoid toplevel collisions
----------------------------
revision 3.565
date: 1995/05/11 22:47:43;   author: dickson;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

avoid toplevel collisions
----------------------------
revision 3.564
date: 1995/05/11 22:46:24;   author: dickson;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.563
date: 1995/05/11 17:19:07;   author: billz;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Replace another flop with orff3 so that UnbHiPriR12 is logically identical
to UnbHiPriR12a.

Present placement should work.  Retrying now.
----------------------------
revision 3.562
date: 1995/05/11 00:53:15;   author: billz;   state: Exp;   lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Here's the change:

< ff_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11)                      ,DB(nbCinR12,
4) );
---
> /* or in D(vldSN128WrtIR11),D(vldSN64WrIQR11) terms to make these cases high
priority */
```

```
> orff3_1 UnbHiPriR12 ( A(phi) ,nbHiPriR11 ,vldSN128WrtIR11 ,vldSN64WrIQR11
,DB(nbCinR12,    4) );
```

The idea is to make vldSN128WrtI and vldSN64WrIQ high priority so they don't
get dropped on the floor in nb. Changed no instance names, so present placement
may work.

Seems to have gotten thru pass2 OK, so I'm releasing it.
----
revision 3.561
date: 1995/05/10 18:49:54; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

attempt to solve top-level routing problems.
----
revision 3.560
date: 1995/05/10 13:32:56; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

this version fully places at the top level
----
revision 3.559
date: 1995/05/09 21:04:38; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisons with xlu
----
revision 3.558
date: 1995/05/09 18:12:01; author: vo; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
      Makefile.tst

Yesterday change to srf rule for the fence wire was messed up . This version
fixed the problem .
----
revision 3.557
date: 1995/05/09 02:28:52; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Makefile.tst:
      Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
      Added this file

uu/Makefile:
      Suppress warning about gdep.in

mc/Makefile:
      Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
      Updated from latest top level

```
----------------------------
revision 3.556
date: 1995/05/08 20:18:13;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce


Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
----------------------------
revision 3.555
date: 1995/05/08 18:24:31;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid collisions with es
----------------------------
revision 3.554
date: 1995/05/07 06:17:59;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc
      mc.power.tab.top

regenerated to reduce strengths no removed from power.tab.local
----------------------------
revision 3.553
date: 1995/05/06 17:10:59;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uu_control.pim uu/uu.power.tab.top \
euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC.  Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ.  The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC.  Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target.  For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc.  Change is to freeze ICC prblm code if target defers prblm.
----------------------------
revision 3.552
date: 1995/05/06 16:18:05;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Yet another placement change.  Should reduce maximum driver to pad
length from ~1.5mm to ~0.5mm.

This converges in 0 iterations with up-to-date drio.power.tab.top.
===============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;   selected revisions: 19
description:
----------------------------
revision 305.0
date: 1995/05/12 02:13:27;  author: stick;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

New file - wingz spreadsheet.
----------------------------
revision 304.7
date: 1995/05/12 02:13:09;  author: stick;  state: Exp;  lines: +6 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 304.6
date: 1995/05/11 23:08:59;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/iq

avoid toplevel collisions
----------------------------
revision 304.5
date: 1995/05/11 22:47:25;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

avoid toplevel collisions
----------------------------
revision 304.4
date: 1995/05/11 22:46:01;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 304.3
date: 1995/05/11 17:18:46;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Replace another flop with orff3 so that UnbHiPriR12 is logically identical
to UnbHiPriR12a.

Present placement should work.  Retrying now.
----------------------------
revision 304.2
date: 1995/05/11 00:52:54;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Here's the change:

< ff_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11)                        ,DB(nbCinR12,
4) );
---
> /* or in D(vldSN128WrtIR11),D(vldSN64WrIQR11) terms to make these cases high
priority */
> orff3_1 UnbHiPriR12 ( A(phi) ,nbHiPriR11 ,vldSN128WrtIR11 ,vldSN64WrIQR11
,DB(nbCinR12,    4) );
```

The idea is to make vldSN128WrtI and vldSN64WrIQ high priority so they don't get dropped on the floor in nb. Changed no instance names, so present placement may work.

Seems to have gotten thru pass2 OK, so I'm releasing it.
----
revision 304.1
date: 1995/05/10 18:49:29; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

attempt to solve top-level routing problems.
----
revision 304.0
date: 1995/05/10 13:32:34; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

this version fully places at the top level
----
revision 303.2
date: 1995/05/09 21:04:21; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisons with xlu
----
revision 303.1
date: 1995/05/09 18:11:40; author: vo; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
      Makefile.tst

Yesterday change to srf rule for the fence wire was messed up . This version
fixed the problem .
----
revision 303.0
date: 1995/05/09 02:28:27; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Makefile.tst:
      Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
      Added this file

uu/Makefile:
      Suppress warning about gdep.in

mc/Makefile:
      Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
      Updated from latest top level
----
revision 302.4

```
date: 1995/05/09 02:28:10;  author: tbr;  state: Exp;  lines: +6 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 302.3
date: 1995/05/08 20:17:52;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce


Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
----------------------------
revision 302.2
date: 1995/05/08 18:24:11;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid collisions with es
----------------------------
revision 302.1
date: 1995/05/07 06:17:38;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc
      mc.power.tab.top

regenerated to reduce strengths no removed from power.tab.local
----------------------------
revision 302.0
date: 1995/05/06 17:10:38;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uu_control.pim uu/uu.power.tab.top \
euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC.  Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ.  The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC.  Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target.  For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc.  Change is to freeze ICC prblm code if target defers prblm.
----------------------------
revision 301.4
date: 1995/05/06 17:10:22;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 301.3
date: 1995/05/06 16:17:43;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Yet another placement change.  Should reduce maximum driver to pad
length from ~1.5mm to ~0.5mm.
```

This converges in 0 iterations with up-to-date drio.power.tab.top.
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 1
description:
----
revision 1.242
date: 1995/05/11 21:41:30;   author: doi;   state: Exp;   lines: +11 -7
put vltree output into a file instead of a make variable (output got too long)
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 3
description:
----
revision 40.78
date: 1995/05/12 00:51:15;   author: tbr;   state: Exp;   lines: +6 -6
set top level MAX_ITERATION to 0
----
revision 40.77
date: 1995/05/09 18:07:58;   author: vo;   state: Exp;   lines: +10 -10
fixed srf rule for fence wire . Signal fence_n was being translated to
xlu/fence_n .
----
revision 40.76
date: 1995/05/08 23:10:53;   author: vo;   state: Exp;   lines: +12 -7
included fence.srf .   This is an acient change that was never commited .
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/cust_intf.list,v
Working file: verilog/bsrc/cust_intf.list
head: 277.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;   selected revisions: 1
description:
----
revision 277.1
date: 1995/05/08 22:02:41;   author: geert;   state: Exp;
Initial check-in of custom interfaces timing data

Geert

```
================================================================================
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cust_intf.wkz,v
Working file: verilog/bsrc/cust_intf.wkz
head: 304.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 304.1
date: 1995/05/12 02:05:48;  author: stick;  state: Exp;
New file - wingz spreadsheet.
================================================================================
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;    selected revisions: 1
description:
----------------------------
revision 6.417
date: 1995/05/06 17:00:00;  author: mws;  state: Exp;  lines: +5 -3
uu/uu.V uu/uu_control.pim euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC.  Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ.  The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC.  Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target.  For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc.  Change is to freeze ICC prblm code if target defers prblm.
================================================================================
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 2
description:
----------------------------
revision 24.71
date: 1995/05/11 07:48:43;  author: mws;  state: Exp;  lines: +52 -3
  Add notes on I & D write/read conflicts and resolution thereof.
  Fix notes on illegal sub-octlet stores.
----------------------------
```

```
revision 24.70
date: 1995/05/11 07:00:22;  author: mws;  state: Exp;  lines: +19 -1
Add note on GTLB NB priority for cache maintenance.
  Add note on BGate(I) updates of privilege level relative to GTLB permissions.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 88.0
date: 1995/05/11 17:18:23;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

Replace another flop with orff3 so that UnbHiPriR12 is logically identical
to UnbHiPriR12a.

Present placement should work.  Retrying now.
----------------------------
revision 87.1
date: 1995/05/11 17:18:15;  author: billz;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 87.0
date: 1995/05/11 00:52:32;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

Here's the change:

< ff_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11)                        ,DB(nbCinR12,
4) );
---
> /* or in D(vldSN128WrtIR11),D(vldSN64WrIQR11) terms to make these cases high
priority */
> orff3_1 UnbHiPriR12 ( A(phi) ,nbHiPriR11 ,vldSN128WrtIR11 ,vldSN64WrIQR11
,DB(nbCinR12,    4) );

The idea is to make vldSN128WrtI and vldSN64WrIQ high priority so they don't
get dropped on the floor in nb.  Changed no instance names, so present placement
may work.

Seems to have gotten thru pass2 OK, so I'm releasing it.
----------------------------
revision 86.1
date: 1995/05/11 00:52:22;  author: billz;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.V,v
Working file: verilog/bsrc/at/at.V
```

```
head: 1.66
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 66;    selected revisions: 4
description:
----------------------------
revision 1.65
date: 1995/05/11 17:17:18;  author: billz;  state: Exp;  lines: +4 -4
Replace another flop with orff3 so that UnbHiPriR12 is logically identical
to UnbHiPriR12a.
----------------------------
revision 1.64
date: 1995/05/11 07:00:45;  author: mws;  state: Exp;  lines: +13 -4
Explain why ifetch loopbacks must be high prio.  Comment only.
----------------------------
revision 1.63
date: 1995/05/11 00:50:35;  author: billz;  state: Exp;  lines: +2 -2
Fixing screw-ups.
----------------------------
revision 1.62
date: 1995/05/10 23:11:11;  author: billz;  state: Exp;  lines: +3 -2
Here's the change:

< ff_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11)                         ,DB(nbCinR12,
4) );
---
> /* or in D(vldSN128WrtIR11),D(vldSN64WrIQR11) terms to make these cases high
priority */
> orff3_1 UnbHiPriR12 ( A(phi) ,D(nbHiPriR11) ,D(vldSN128WrtIR11)
,D(vldSN64WrIQR11) ,DB(nbCi
nR12,    4) );

The idea is to make vldSN128WrtI and vldSN64WrIQ high priority so they don't
get dropped on the floor in nb.  Changed no instance names, so present placement
may work. I'll let 'er rip and find out.
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 80.0
date: 1995/05/12 02:07:11;  author: stick;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

New file - wingz spreadsheet.
----------------------------
revision 79.1
```

```
date: 1995/05/12 02:07:03;  author: stick;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 79.0
date: 1995/05/08 20:17:31;  author: vo;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/ce


Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
----------------------------
revision 78.1
date: 1995/05/08 20:17:24;  author: vo;  state: Exp;  lines: +17 -17
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/Makefile.gards,v
Working file: verilog/bsrc/ce/Makefile.gards
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 1.15
date: 1995/05/08 20:15:40;  author: vo;  state: Exp;  lines: +8 -8
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_cms2ecl.V,v
Working file: verilog/bsrc/ce/ce_cms2ecl.V
head: 2.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
description:
----------------------------
revision 2.18
date: 1995/05/08 20:15:43;  author: vo;  state: Exp;  lines: +38 -19
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
```

```
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_flash.V,v
Working file: verilog/bsrc/ce/ce_flash.V
head: 2.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
----------------------------
revision 2.19
date: 1995/05/08 20:15:46;  author: vo;  state: Exp;  lines: +8 -8
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_mck.V,v
Working file: verilog/bsrc/ce/ce_mck.V
head: 32.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 32.12
date: 1995/05/08 20:15:49;  author: vo;  state: Exp;  lines: +1 -0
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_seg7.V,v
Working file: verilog/bsrc/ce/ce_seg7.V
head: 2.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 2.10
date: 1995/05/08 20:15:51;  author: vo;  state: Exp;  lines: +9 -6
Many random slow node fixes  plus :
```

```
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
===============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cecore.V,v
Working file: verilog/bsrc/ce/cecore.V
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 1
description:
----------------------------
revision 1.24
date: 1995/05/08 20:15:54;  author: vo;  state: Exp;  lines: +120 -154
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
===============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cemaster.V,v
Working file: verilog/bsrc/ce/cemaster.V
head: 1.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 1.13
date: 1995/05/08 20:15:58;  author: vo;  state: Exp;  lines: +69 -61
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
===============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
----------------------------
```

```
revision 1.54
date: 1995/05/08 20:16:02;  author: vo;  state: Exp;  lines: +2 -2
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.cpif,v
Working file: verilog/bsrc/ce/cerberus.cpif
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
----------------------------
revision 1.29
date: 1995/05/11 17:18:59;  author: vo;  state: Exp;  lines: +175 -175
improved for routability at the top level .
----------------------------
revision 1.28
date: 1995/05/08 20:16:23;  author: vo;  state: Exp;  lines: +6562 -6323
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbnobreg.V,v
Working file: verilog/bsrc/ce/cerbnobreg.V
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;    selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/05/08 20:16:43;  author: vo;  state: Exp;  lines: +13 -11
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbskewreg.V,v
Working file: verilog/bsrc/ce/cerbskewreg.V
head: 1.6
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/05/08 20:16:44;  author: vo;  state: Exp;  lines: +80 -2
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtempreg.V,v
Working file: verilog/bsrc/ce/cerbtempreg.V
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 1
description:
----------------------------
revision 1.9
date: 1995/05/08 20:16:46;  author: vo;  state: Exp;  lines: +82 -44
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;     selected revisions: 1
description:
----------------------------
revision 1.41
date: 1995/05/08 20:16:48;  author: vo;  state: Exp;  lines: +6 -2
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
================================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceregcore.V,v
Working file: verilog/bsrc/ce/ceregcore.V
head: 1.44
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 44;    selected revisions: 1
description:
----------------------------
revision 1.41
date: 1995/05/08 20:16:50;  author: vo;  state: Exp;  lines: +42 -30
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceslave.V,v
Working file: verilog/bsrc/ce/ceslave.V
head: 1.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
----------------------------
revision 1.20
date: 1995/05/08 20:16:52;  author: vo;  state: Exp;  lines: +356 -475
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
cerberus.cpif: moved owdata converters closer to the rhs boundary +
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/pimlib.pl,v
Working file: verilog/bsrc/ce/pimlib.pl
head: 77.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;    selected revisions: 1
description:
----------------------------
revision 77.4
date: 1995/05/08 20:16:54;  author: vo;  state: Exp;  lines: +293 -24
Many random slow node fixes  plus :
ceslave.V : regrouped, renamed similar gates to facililate placement by script
cerbskewreg.V : double size of control drivers for octlet32,33 . These octlets
are
                more scattered than the rest .
```

cerberus.cpif: moved owdata converters closer to the rhs boundary +
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v
Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;   selected revisions: 2
description:
releasebom adding BOM
----
revision 34.0
date: 1995/05/11 22:47:05; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/gf

avoid toplevel collisions
----
revision 33.1
date: 1995/05/11 22:46:54; author: dickson; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/clean-request,v
Working file: verilog/bsrc/gf/clean-request
head: 11.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;   selected revisions: 1
description:
----
revision 11.8
date: 1995/05/11 22:45:55; author: dickson; state: Exp; lines: +1 -0
avoid toplevel collisons
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.pim,v
Working file: verilog/bsrc/gf/gf.pim
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;   selected revisions: 1
description:
----
revision 4.12
date: 1995/05/11 22:45:59; author: dickson; state: Exp; lines: +8 -8
avoid toplevel collisons
==

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM

```
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 46.0
date: 1995/05/06 17:06:43;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uu_control.pim uu/uu.power.tab.top \
euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC.  Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ.  The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC.  Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target.  For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc.  Change is to freeze ICC prblm code if target defers prblm.
----------------------------
revision 45.1
date: 1995/05/06 17:06:35;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/BOM,v
Working file: verilog/bsrc/iq/BOM
head: 67.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 145;   selected revisions: 2
description:
----------------------------
revision 67.0
date: 1995/05/11 23:08:39;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/iq

avoid toplevel collisions
----------------------------
revision 66.1
date: 1995/05/11 23:08:31;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/clean-request,v
Working file: verilog/bsrc/iq/clean-request
head: 24.8
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
----------------------------
revision 24.8
date: 1995/05/11 23:07:50;  author: dickson;  state: Exp;  lines: +2 -1
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/iq.pim,v
Working file: verilog/bsrc/iq/iq.pim
head: 61.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 1
description:
----------------------------
revision 61.2
date: 1995/05/11 23:07:52;  author: dickson;  state: Exp;  lines: +32 -32
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v
Working file: verilog/bsrc/mc/BOM
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;    selected revisions: 7
description:
releasebom adding BOM
----------------------------
revision 76.0
date: 1995/05/09 21:04:02;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisons with xlu
----------------------------
revision 75.1
date: 1995/05/09 21:03:55;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 75.0
date: 1995/05/09 02:24:23;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile.tst:
     Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
     Added this file
```

```
uu/Makefile:
      Suppress warning about gdep.in

mc/Makefile:
      Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
      Updated from latest top level
--------------------------
revision 74.1
date: 1995/05/09 02:24:15;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
--------------------------
revision 74.0
date: 1995/05/08 18:23:48;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

avoid collisions with es
--------------------------
revision 73.2
date: 1995/05/08 18:23:39;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
--------------------------
revision 73.1
date: 1995/05/07 06:17:17;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc
      mc.power.tab.top

regenerated to reduce strengths no removed from power.tab.local
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/Makefile,v
Working file: verilog/bsrc/mc/Makefile
head: 1.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
--------------------------
revision 1.20
date: 1995/05/08 21:32:18;  author: tbr;  state: Exp;  lines: +1 -3
remove explicit GARDS_DISPLAY setting
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/clean-request,v
Working file: verilog/bsrc/mc/clean-request
head: 17.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 2
```

```
description:
----------------------------
revision 17.19
date: 1995/05/09 21:03:03;  author: dickson;  state: Exp;  lines: +2 -1
avoid toplevel collisions with xlu
----------------------------
revision 17.18
date: 1995/05/08 18:22:45;  author: dickson;  state: Exp;  lines: +2 -1
move mc to right to avoid collisions with es
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/genpim.pl,v
Working file: verilog/bsrc/mc/genpim.pl
head: 13.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 13.15
date: 1995/05/08 18:22:46;  author: dickson;  state: Exp;  lines: +3 -3
move mc to right to avoid collisions with es
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataHigh.pim,v
Working file: verilog/bsrc/mc/mc.dataHigh.pim
head: 48.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 48.8
date: 1995/05/09 21:03:06;  author: dickson;  state: Exp;  lines: +304 -304
avoid toplevel collisions with xlu
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.power.tab.top,v
Working file: verilog/bsrc/mc/mc.power.tab.top
head: 37.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 37.11
date: 1995/05/07 06:16:50;  author: tbr;  state: Exp;  lines: +955 -827
regenerated to reduce strengths no removed from power.tab.local
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
```

```
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 4
description:
----------------------------
revision 126.0
date: 1995/05/11 22:45:36;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 125.1
date: 1995/05/11 22:45:26;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 125.0
date: 1995/05/09 02:25:45;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile.tst:
      Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
      Added this file

uu/Makefile:
      Suppress warning about gdep.in

mc/Makefile:
      Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
      Updated from latest top level
----------------------------
revision 124.1
date: 1995/05/09 02:25:36;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/clean-request,v
Working file: verilog/bsrc/rg/clean-request
head: 60.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
```

```
revision 60.12
date: 1995/05/11 22:44:40;  author: dickson;  state: Exp;  lines: +1 -0
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/genptab.pl,v
Working file: verilog/bsrc/rg/genptab.pl
head: 82.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 82.2
date: 1995/05/11 22:44:42;  author: dickson;  state: Exp;  lines: +8 -8
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/Attic/power.tab.local,v
Working file: verilog/bsrc/rg/power.tab.local
head: 19.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 19.3
date: 1995/05/11 22:44:44;  author: dickson;  state: Exp;  lines: +390 -390
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 1
description:
----------------------------
revision 82.23
date: 1995/05/09 02:14:44;  author: tbr;  state: Exp;  lines: +3 -3
Moved 3 cells to prevent overlap.  updated power.tab.top
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.power.tab.top,v
Working file: verilog/bsrc/rg/rg.power.tab.top
head: 79.12
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 79.11
date: 1995/05/09 02:15:38;  author: tbr;  state: Exp;  lines: +118 -118
Moved 3 cells to prevent overlap.  updated power.tab.top
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 6
description:
----------------------------
revision 197.0
date: 1995/05/10 18:49:04;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

attempt to solve top-level routing problems.
----------------------------
revision 196.1
date: 1995/05/10 18:48:52;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 196.0
date: 1995/05/09 02:26:56;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile.tst:
      Include fence.srf where appropriate - vo can say what it does!

cust_inst.list:
      Added this file

uu/Makefile:
      Suppress warning about gdep.in

mc/Makefile:
      Remove explicit GARDS_DISPLAY setting

rg/rg.pim:
      Moved 3 cellt to prevent overlap with gf

rg/rg.power.tab.top:
      Updated from latest top level
----------------------------
revision 195.1
date: 1995/05/09 02:26:46;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 195.0
date: 1995/05/06 17:09:23;  author: mws;  state: Exp;  lines: +1 -1
```

Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uu_control.pim uu/uu.power.tab.top \
euterpe.V icc/icc.V icc/icc.pim.txt:
  UU used the frozen ICC problem code to decide exceptions and hiccups (and
  preempts) from IFetch/ICC. Mostly this is fine, as ICC will generate
  exceptions and freeze its code, and send validation fully pipelined to UU
  thru IQ. The risk is in the deferred branch target exception case, for which
  the ifetch problem status does not originate in ICC. Then ICC's code is not
  frozen, but follow-on sequential ifetching could pick up a seqntial-new-page,
  ITag miss, etc., and change the code to a value inconsistent with what UU
  expects for the target. For example, an ITag detail/CC/disallow could be
  reported from a following instruction if the GTLB is rewritten to remove
  a miss, etc. Change is to freeze ICC prblm code if target defers prblm.
----
revision 194.1
date: 1995/05/06 17:09:14; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
===

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/Makefile,v
Working file: verilog/bsrc/uu/Makefile
head: 1.79
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79;   selected revisions: 1
description:
----
revision 1.78
date: 1995/05/06 17:52:23; author: tbr; state: Exp; lines: +6 -3
suppress warning about not being able to open gdep.in
===

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;   selected revisions: 1
description:
----
revision 68.49
date: 1995/05/10 18:46:14; author: woody; state: Exp; lines: +5305 -4238
attempt to solve top-level routing problems.
===